Description

BACKGROUND-CALIBRATING PIPELINED ANALOG-TO-DIGITAL CONVERTER

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to digital electronics, and more specifically, to a background calibrating pipelined analog-to-digital converter.

[0003] 2. Description of the Prior Art

[0004] Pipelined analog-to-digital converters (ADCs) are widely used in applications such as video imaging systems, digital subscriber loops, Gigabit Ethernet transceivers, and wireless communications. Pipelined analog-to-digital (A/D) conversion offers a good trade-off among power, speed, and integrated circuit die area, and is suitable for implementing high-resolution ADCs operating at sampling frequencies in the order of megahertz.

[0005] Fig.1 illustrates a state-of-the-art pipelined ADC 10. The

ADC 10 includes a series of multiplying digital-to-analog converter (MDAC) stages 12, 14, 16, which may or may not be identical, and an encoder 18. The first MDAC stage 12 receives an analog signal V_1 and outputs a digital code D_1 representative of the analog signal V_1 according to a predefined precision. Successive stages 14, 16 output digital codes D_2, D_3 according to successive amplified residual signals V_2, V_3 of the first and second stages 12, 14 respectively. Each successive stage digitizes the residue of the previous stage, so accordingly, the digital output D_1 of the first stage 12 contains the most significant bits (MSBs) while the output D_P of the last stage 16 contains the least significant bits (LSBs). The encoder 18 arranges the outputs D_1, D_2, D_3 of the stages 12, 14, 16 to produce a consistent digital representation D_0 of the input analog signal V_1.

[0006] Fig.2 illustrates a typical MDAC 20 used for the MDAC stages 12, 14, 16 of the ADC 10 of Fig.1. The MDAC 20 includes an internal ADC 22, a digital-to-analog converter (DAC) 24, an adder 26, and an amplifier 28. In operation, an analog input V_j received from a previous stage (or as an input signal itself) is quantized by the ADC 22 producing a digital code D_j that is an estimation of V_j. The DAC 24

generates a corresponding analog signal $V_j^{da}(D_j)$ that is then subtracted from the input signal V_j by the adder 26. The residue outputted by the adder 26 is amplified by the amplifier 28 according to a gain factor G_j. The output V_{j+1} of the MDAC 20 can be described as follows:

$$V_{j+1} = G_j \times [V_j - V_j^{da}(D_j)] \tag{1}$$

Accordingly, the input of the pipelined ADC 10 can then be expressed as:

$$V_1 = V_1^{da} + \frac{V_2^{da}}{G_1} + \frac{V_3^{da}}{G_1 G_2} + \cdots + \frac{V_p^{da}}{G_1 G_2 \cdots G_{p-1}} + Q \qquad (2)$$

[0007]   where $Q = V_{P+1}/(G_1 G_2 \ldots G_P)$ is the quantizing error of the entire A/D conversion. The encoder 18 of Fig.1 calculates the digital output D_0 by subtracting Q from V_1. The signals V_j^{da} and gains G_j are design parameters. In addition, it is well known that the conversion characteristics of the internal ADC 22 in the pipeline stages 20 have no effect on the digital output D_0.

[0008]   In CMOS applications, most A/D pipeline stages are realized with switched-capacitor (SC) MDACs, which include comparators, operational amplifiers (opamps), switches, and capacitors as described above. Fig.3 shows a prior art radix-2 1.5 bit SC MDAC 30 having a conversion charac-

teristic as illustrated in Fig.4. The MDAC 30 includes comparators 32, 34, an encoder 36, switches 38, first and second capacitors 40, 42 having respective capacitances C_f and C_s, and an operational amplifier 44. During a sample phase, when a first clock is high, the switches 38 marked 1 are exclusively closed, and the signal V_j is sampled on the first and second capacitors 40, 42. Accordingly, the digital code output is determined as-1, 0, or +1 according to the comparators 32, 34 comparing the signal V_j with +0.25V_r and -0.25V_r references respectively. Conversely, during a hold phase, when a second clock is high, the switches 38 marked 2 are exclusively closed. During the hold phase, the output V_{j+1} can be expressed as:

$$V_{rH} = \left(1 + \frac{C_s}{C_f}\right) \times \left[V_j - \frac{C_s}{C_s + C_f} V_r \cdot D_j\right] \qquad (3)$$

[0009] assuming linear behavior of the capacitors 40, 42, and an ideal operational amplifier 44 with infinite DC gain and zero input offset voltage.

[0010] In practical application, the capacitances C_f and C_s of the capacitors 40, 42 are desired to be the same. However, due to capacitance mismatches (C_f not equal to C_s) and input offset voltage of the operational amplifier 44 in implementation, the pipelined ADC 10 must be calibrated for accurate results.

[0011] Regarding calibration, there is a fundamental trade-off between ADC operation speed and accuracy, which depends on the matching properties of devices such as

MOSFETs and capacitors. The accuracy of an MDAC is dictated by the input offset voltages of the comparators and the operational amplifier, and the exact values of the capacitor ratios. To overcome this speed-accuracy trade-off, several self-calibration techniques have been developed. Although the calibration can be performed in the analog domain, entirely digital approaches are preferred in deep sub-micron technologies, due to reduced cost of added digital circuitry. In addition, in digital self-calibration schemes the necessary modification to the MDACs is non-critical, and thus, the analog signal paths suffer little performance degradation.

[0012] Conventional self-calibration schemes require reconfiguration of MDACs, which cannot be performed without interrupting normal A/D operation. Thus, in applications that can afford little idle time, ADCs are calibrated only during an initial power-on state. Any power-on calibration may later become invalid because of variations in supply voltage and temperature. To address this problem, several background calibration schemes have been developed that enable an ADC to continuously calibrate internal MDACs to track environmental changes while simultaneously performing normal conversion without resolution degrada-

tion.

[0013] There are several well-known approaches to background calibration. The "skip-and-fill" algorithm randomly skips A/D cycles to calibrate the MDACs and fill in the missing outputs by nonlinear interpolation, as described in U.K. Moon and B.S. Song, "Background digital calibration techniques for pipelined ADCs", *IEEE Trans. Circuits Syst. II*, vol.44, pp.102-109, February 1997 and S.U. Kwak, B.S. Song, and K. Bacrania, "A 15-b, 5-Msample/s low-spurious CMOS ADC", *IEEE J. Solid-State Circuits*, vol.32, pp.1866-1875, December 1997, which are incorporated herein by reference. However, the bandwidth of the input signal needs to be limited for the interpolator to achieve good results. Moreover, if a multi-bit MDAC is used in a pipeline stage, it is possible to estimate the MDACs conversion errors in normal A/D operation using information on the MDACs mismatch pattern. But, without the MDACs gain error information, this approach is only suitable for high gain pipeline stages.

[0014] Background calibration can also be achieved by using an extra MDAC to replace the one under calibration, as described in J.M. Ingino and B.A. Wooley, "A continuously calibrated 12-b, 10-MS/s, 3.3V A/D converter", *IEEE J.*

Solid-State Circuits, vol.33, pp.1920-1931, December 1998, which is incorporated herein by reference. However, the complexity of the required analog switching scheme can degrade speed performance of the analog signal path.

[0015] Another scheme proposed in J.Ming and S.H. Lewis, "An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration,"*IEEE J. Solid-State Circuits*, vol.36, pp.1489-1497, October 2001, which is incorporated herein by reference, is only capable of correcting gain error while adding significant analog and digital hardware.

[0016] Finally, an example of a self-calibrating reversible pipeline ADC/DAC is disclosed in US 5,929,796, which is incorporated herein by reference.

[0017] The conventional background calibration schemes are in need of improvement with respect to nonlinear effects due to MDAC gain error, input offset voltage, and output errors in the digital-to-analog conversion.

SUMMARY OF INVENTION

[0018] It is therefore a primary objective of the claimed invention to provide an MDAC stage, a background-calibrating pipelined ADC, and a related method to overcome the above-described shortcomings of the prior art.

[0019]   Briefly summarized, an MDAC stage according tothe
claimed invention includes a sub-analog-to-digital con-
verter for converting an analog signal received at an input
node to a digital code, an amplifier, and a first capaci-
tance selectively connected between the input node and
the amplifier input and between the amplifier input and
the amplifier output. The claimed MDAC further includes a
plurality of second capacitances connected in parallel se-
lectively between the input node and the amplifier input
and between a corresponding plurality of digital reference
signals and the amplifier input. The plurality of digital ref-
erence signals comprises digital signals corresponding to
the digital code and a first calibration signal. During a
sample phase the first capacitance is connected between
the input node and the amplifierinput and the plurality of
second capacitances are connected in parallel between the
input node and the amplifier input. During a hold phase
the first capacitance is connected between the amplifier
input and the amplifieroutput and the plurality of second
capacitances are connected in parallel between the plural-
ity of digital reference signals and the amplifier input.

[0020]   According to the claimed invention, a pipelined ADC in-
corporating a series of claimed MDAC stages includes a

multiplier connected to the output of the last MDAC stage of the series. The multiplier is capable of determining a product of the last MDAC stage output anda second calibration signal corresponding to the first calibration signal. Further provided are a low-pass filterconnected to the multiplier for filtering output of the multiplier and outputting a DC component, and an encoder for receiving output of the MDAC stages and generating a digital output signal, and for compensating the digital output signal with the DC component.

[0021] According to the claimed invention, a method includes steps of sampling an input analog signal on a first capacitance and a plurality of second capacitances of an MDAC stage during a sample phase, applying a first calibration signal to a second capacitance of the MDAC stage during a hold phase, and finally, filtering the first calibration signal from the digital output of the pipelined analog-to-digital converter.

[0022] It is an advantage of the claimed invention that the plurality of second capacitances and the first calibration signal allow for calibration without interruption of normal A/D conversion.

[0023] It is a further advantage of the claimed invention that the

plurality of second capacitors results in no significant extra capacitive loads so that operating speed is not degraded.

[0024] It is a further advantage of the claimed invention that nonlinear effects due to gain error, input offset voltage, and output errors in the digital-to-analog conversion are reduced.

[0025] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0026] Fig.1 is a block diagram of a prior art pipelined ADC.

[0027] Fig.2 is a block diagram of a prior art MDAC for the ADC of Fig.1.

[0028] Fig.3 is a block diagram of a prior art radix-2 1.5 bit SC MDAC.

[0029] Fig.4 is a graph of a conversion characteristic of a radix-2 1.5 bit SC MDAC.

[0030] Fig.5 is a block diagram of a radix-2 1.5 bit SC MDAC according to the present invention.

[0031]   Fig.6 is a block diagram of pipelined MDACs of Fig.5.

[0032]   Fig.7 is a block diagram of a pipelined ADC according to the present invention.

[0033]   Fig.8 is a graph of the effects of the low-pass filters of Fig.6 and Fig.7.

[0034]   Fig.9 is a graph of transient behaviors for low-pass filter designs according to the present invention.

[0035]   Fig.10 is a graph of SNDR of the output of an ADC according to the present invention operated at different input frequencies.

DETAILED DESCRIPTION

[0036]   Please refer to Fig.5 illustrating a block diagram of an MDAC 50 according to the present invention. The MDAC 50 is illustrated as a radix-2 1.5 bit SC MDAC, however, the present invention applies to other types of pipeline stages, such as those having multi-bit operation without switched capacitors.

[0037]   The MDAC 50 includes a sub-ADC 52 for converting an input analog signal V_j to a digital code D_j. The sub-ADC 52 includes comparators 54, 56 and an encoder 58 capable of producing 1.5 bit output, such as 00, "01, or 10, utilizing a reference voltage V_r. Detailed design and oper-

ation of the sub-ADC 52 is well known in the art. The MDAC 50 further comprises a plurality of switches 60 selectively connecting a first capacitor 62, and second capacitors 64, 66, 68 between the sub-ADC 52, the input analog signal V_j, and an amplifier 70. The second capacitors 64, 66, 68 are arranged in parallel and are capable of sharing the same input and output. The switches 60 can be realized with typical switching devices such as transistors. Each switch 60 closes and opens according to the operational phase of the MDAC 50. That is, switches marked with a 1 in Fig.5 are exclusively closed during a sample phase, while switches marked with a 2 are exclusively closed during a hold phase. The first capacitor 62 has a capacitance of C_f, and the second capacitors 64, 66, 68 have capacitances of $C_{s,1}$, $C_{s,i}$, $C_{s,N}$ respectively. Although, only three second capacitors 64, 66, 68 are illustrated, the present invention requires simply a minimum of two second capacitors, with a maximum of as many as practical. The sum of capacitances of all second capacitors 64, 66, 68 used in the MDAC 50 should be selected as nominally equal to the capacitance of the first capacitor 62 such that:

$$C_f \approx C_{s,1} + C_{s,2} + \cdots + C_{s,N} \qquad (4)$$

[0038]   In operation, during the sample phase, the switches 60
are set such that all capacitors 62, 64, 66, 68 are con-
nected to sample the input signal V_j. Conversely, during
the hold phase, the switches 60 are set such that second
capacitors 64, 68 are connected to the reference voltage V
$_r$ multiplied by the determined digital code D_j, while a se-
lected second capacitor 66 can be connected to a first cal-
ibration signal, which is the reference voltage V$_r$ multiplied
by a pseudo-random digital binary-valued sequence q.
Whether any second capacitance receives the first calibra-
tion digital depends on if it is under calibration. The basis
of selecting which second capacitor is to receive the first

calibration signal should be sound design principles or otherwise whatever choice is convenient, as all second capacitors should eventually individually receive the first calibration signal. The sequence q alternates between +1 and 0 or between -1 and 0 depending on the digital code output D_j as being a 1 or -1 respectively. As such, output V_{j+1} of the MDAC 50 can be expressed as:

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{do}(D_j) + \frac{C_{s,i}}{C_f} V_r \cdot D_j - \frac{C_{s,i}}{C_f} V_r \cdot q \right] \qquad (5)$$

where the actual gain of the amplifier 70 is

$$\hat{G}_i = 1 + C_s/C_r, C_L = C_s + C_r$$

, and the actual analog signal generated based on the digital code D_j is:

$$\hat{G}_i = 1 + C_s/C_r, C_L = C_s + C_r$$

$$\hat{V}_i^{do}(D_i) = \frac{C_s}{C_s + C_f} V_r \cdot D_i = \frac{\sum_{n=1}^{N} C_{s,n}}{C_f} V_r \cdot D_i \qquad (6)$$

[0039] How the random signal q is applied to the second capacitors 64, 66, 68 to effect background calibration is further described referencing Fig.6, which illustrates a simplified (for purposes of explanation) ADC 80 incorporating the MDAC stage 50. When a plurality of MDAC stages 50 are connected in series to realize an ADC, such as the ADC 10 of Fig.1, when considering operations of a particular stage, further LSB stage can be consolidated for simplification. Accordingly, the ADC 80 includes an MDAC 50, a z-ADC 82 representing the combined LSB stages, a multiplier 89 for combining the output D_z of the z-ADC 82 with a second calibration signal q corresponding to the first

calibration signal q, a low-pass filter 86 for obtaining the DC component of the output $q \cdot D_z$ of the multiplier 89, and an encoder 88.

[0040] Generally, during operating, the random calibration signal q is injected into the second capacitors 64, 66, 68 of the MDAC 50, and removed from the digital output D_j of the MDAC 50 and the digital output D_z of the z-ADC 82 at the encoder 88. This is facilitated by selecting the random sequence q as having the same waveform pattern as the random calibration sequence q, however, with values alternating between +1 and -1 (i.e. has zero DC component).

[0041] The MDAC 50 and ADC 80 inherently perform the following mathematical description, which is presented simply for a better understanding of the present invention. The value of fromequation (5) is estimated by quantizing V_{j+1} using the z-ADC 82, and then low pass filtering the product $q \cdot D_z$ in the digital domain with the low-pass filter 86. If the signal q has a mean value very close to 0, and is uncorrelated with V_j, then the DC component of the product $q \cdot D_z$ corresponds to the gain error of the z-ADC 82 by

$$D_{\Delta} = \Delta_i \hat{G}_t / G_{\tau}, \text{'}$$

where:

$$D_{\Delta} = \Delta_i \hat{G}_t / G_{\tau}, \text{'}$$

$$\Delta_i = -\overline{q^i q} \times \hat{G}_j \, \frac{C_{3,i}}{C_i} V_r = -\frac{1}{2} \hat{G}_j \, \frac{C_{3,i}}{C_i} V_r \qquad (7)$$

And, by combining equations (6) and (7) above:

$$\hat{G}_j \times \hat{V}_j^{dn}(D_j) = -2 \cdot D_j \times \sum_{i=1}^{N} \Delta_i \qquad (8)$$

Then, once the term

$\hat{G}_j V_j^{de}(D_j)$

for equation (8) is obtained for all values of D_j, the result $T_j(D_j)$ is determined as:

$$T_j(D_j) = \frac{D_z(D_j)}{G_j} \qquad\qquad (9)$$

For normal A/D operation of the ADC 80, the digital output D_0 of the encoder 88 is D_{jz} as below:

$$\text{Digital Output} = D_{jz} = T_j(D_j) + \frac{D_z}{G_j}$$ (10)

Note that the raw digital output D_z of the z–ADC 82 includes the last two terms of equation (5), which must be subtracted from D_z before calculating D_{jz}. Once

of equation (7) has converged, these two noise terms can be calculated with high precision and completely removed from D_z. Also note that in the above mathematical description, intermediate and supporting equations have been omitted for conciseness, however, these are well known to those knowledgeable in theories of digital calibration.

[0042] As a result, the voltage range for the output V_{j+1} according to the present invention can be expressed as:

$$\left|V_{j+1}\right| \leq V_r \times \left(\frac{C_s + C_f}{4C_f} + \frac{C_{s,i}}{C_f} \right) \qquad (11)$$

assuming that the comparators 54, 56 of Fig.5 are ideal and the input V_j is bounded between $\pm V_r$. As the present invention background calibration adds the random signal q into the output V_{j+1}, extra voltage range is required as indicated by the $C_{s,i}/C_f$ term in equation (11). Thus, it is desirable to select a smaller combined capacitance C_s for the second capacitors 64, 66, 68, or to use a larger number of second capacitors.

[0043] Please refer to Fig.7, illustrating an ADC 90 as practically implemented according to the present invention. The ADC 90 includes a series of MDAC stages 92, 94, 96, which are identical to the present invention MDAC stage 50. Similar

to the ADC 80, the ADC 90 also comprises a multiplier 97, a low-pass filter 98, and an encoder 100. The ADC 90 further comprises a pseudo-random signal generator 102 for generating the signals q, q, and a memory 104 for storing the DC component of the output

D_A

of the multiplier 97. Three MDAC stages 92, 94, 96 are shown, however, more or fewer are acceptable.

[0044] During A/D conversion operation of the ADC 90, an external analog signal V_1 is input into the first MDAC stage 92. The first MDAC stage 92 generates a corresponding digital code D_1, and outputs a residue analog signal V_2 to the second MDAC stage 94. This is continuously repeated

according to sample and hold phases for all MDAC stages 92, 94, 96, with digital codes D_1, D_2, D_p corresponding to the input analog signal V_1 being output to the encoder 100. To achieve calibration, the pseudo-random signal generator 102 generates the random calibration sequence q and progressively injects it into the second capacitors 64, 66, 68 (see Fig.5) of the MDACs stages 92, 94, 96, beginning with the least significant bit MDAC to be calibrated and progressing to the most significant bit MDAC to be calibrated. The order in which the second capacitors 64, 66, 68 receive the signal q is unimportant, however, the LSB to MSB calibration order of the stages 92, 94, 96 should be maintained. To compensate for the random first calibration signal q, the pseudo random signal generator 102 also applies the corresponding second calibration signal q to the output of the last stage 96 of the ADC 90. The DC component

D_1

of this result is then produced by the low-pass filter 98,

which outputs the DC component

D_1

to the encoder 100 and the memory 104. Finally, the en-

coder 100, supported by data in the memory 104, re-

moves traces of the input random calibration sequence q

to output the calibrated digital signal D_0.

[0045] Fig.8 illustrates the effects of the low-pass filters 86, 98

of Fig.6 and Fig.7 when used to extract Equation.

Δ,

from white noise W when suitably designed by one skilled in the art. The low-pass filters 86, 98 can be of typical designs, or can also be decimation filters, provided they are compatible with the above description of the present invention.

[0046] Simulations have been performed to demonstrate the benefits of the present invention background calibration. Referring back to Fig.6, a simulated pipelined ADC was given an MDAC stage 50 followed by an ideal 17-bit z-ADC 82. The MDAC stage 50 was set with a non-ideal capacitor ratio of $C_s/C_f = 0.98$ (2% mismatch) and an offset $V^{OS} = 0.01V_r$. The MDAC stage 50 was given four second

capacitors (N=4) of equal capacitance. The input signal V_j was a sinusoidal signal with $0.5V_r$ amplitude and a frequency of approximately 2/5 the sampling frequency. When the MDAC 50 was left uncalibrated the signal-to-noise-and-distortion ratio (SNDR) was measured as 43.4 dB, and the spurious-free dynamic range (SFDR) was 47.2 dB, resulting in aneffective number of bits (ENOB) of 6.9 bits. When the present inventionbackground calibration was applied with a well-designed low-pass filter 86 having $\mu = 2^{-28}$, the SNDR became 92.7 dB and the SFDR became 99.6 dB, resulting in an ENOB of 15.1 bits. When different μ values were applied to the low-pass filter 86, transient behaviors were as illustrated in Fig.9, which shows that using a smaller μ value (for good resolution) requires a longer time for convergence. When the low-pass filter was replaced with a suitably designed decimation filter having an $M = 2^{28}$, the SNDR was 88.0 dB, and the SFDR was 90.2 dB, resulting in an ENOB of 14.3 bits.

[0047] Fig.10 shows SNDR of the output of the simulated ADC at different input frequencies. The ADC was separately calibrated using both the previously described low-pass filter, as indicated by curve 110, and the decimation filter, as indicated by curve 112.

[0048] In contrast to the prior art, the present invention MDAC includes a plurality of second capacitances that are provided with a random calibration signal. The present invention MDAC, ADC, and method are capable of simultaneous calibration and A/D conversion. The present invention requires only a small modification of the analog signal path, and does not degrade operating speed, and further, reduces nonlinear effects due to capacitor mismatches, DC offset voltage, and reference voltage inaccuracy.

[0049] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.